REMARKS

By the foregoing amendment, claims 1 to17 have been canceled and claims 18 to 35 have been added. Claims 18 to 35 are pending in the application. The amendments have been made to render the claims even more in conformance with U.S. patent practice and to further clarify the claimed inventions. No new matter has been added and support for the amendments can be found throughout the application. Entry of the above amendment is respectfully requested.

Telephone Interview with the Examiner

Applicants thank the Examiner for a telephone interview on March 10, 2008 with Applicants' representative. The Action states that claims 1, 4, and 13 (actually 1, 4, and 14) are rejected under 35 U.S.C. § 103(a). During the telephone conversation, the Examiner confirmed that the rejection of claim 13 under § 103(a) was an inadvertent typographical error and that claim 14 was originally intended. Therefore, this response will not address the obviousness rejection of claim 13.

Formal Matters

Applicants thank the Examiner for considering the documents submitted in the Information Disclosure Statement of June 14, 2006 by returning a signed and initialed copy of the Form PTO-1449.

Applicants also note with appreciation that the Office Action acknowledges the claim for foreign priority under 35 U.S.C. § 119 and confirms that the Office received all copies of the certified copies of the priority documents.

It is also noted with appreciation that the Office accepts the drawings filed in the application on March 26, 2006.

Specification

The Examiner has requested that the Applicants correct any errors in the specification of which Applicants may become aware. In this regard, Applicants have again reviewed the specification and have not become aware of any errors therein.

Claim Rejections under § 112

The Action rejects claims 2, 3, 5, 6, 8-13, and 15-17 under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the enablement requirement. More specifically, the Action asserts that one of skilled in the art would not know what is meant by "old ASTM" as guidelines for interstitial oxygen content in semiconductor materials.

Applicants respectfully traverse this rejection. Applicants note that it is well-known in the art what is meant by the term "old ASTM" as oppose to "new ASTM." As evidence, Applicants submit an excerpt from the following textbook:

Fumio SHIMURA, "Semiconductor and Silicon Crystal Technology", Academic Press, Inc., San Diego, New York, Berkeley, Boston, London, Sydney, Tokyo, Toronto, 1989, pp. ii-viii, 1, 232-233, and 274-275; Applicants note that a Form PTO-1449 listing this document is enclosed.

On page 233, the reference explains explicitly the difference between "old ASTM" and "new ASTM." In view of these remarks, withdrawal of this rejection is respectfully requested.

The Action rejects claims 1-17 under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite. The Examiner asserts that the claims appear to be a literal translation and contain grammatical and idiomatic errors. For examination purposes, the Examiner has treated the claims as though there is only one SOI wafer with an active layer and a supportive layer.

In view of the foregoing, Applicants submit that the claims have been rewritten to render them even closer in conformance with idiomatic English and U.S. Patent practice. Withdrawal of this rejection is respectfully requested.

Claim Rejections under 35 U.S.C § 103(a)

The Action rejects claims 1, 4, and 14 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Tamatsuka et al. (U.S. Patent No. 6,224,668 B1) in view of Falster et al. (U.S. Patent Application Publication No. 2005/0255671 A1). The Office asserts that Tamatsuka discloses the recitations of claims 1, 4, and 14 with the exception of "oxidation induced stacking faults," for which Falster allegedly provides the requisite disclosure.

Initially, Applicants respectfully submit that claims 1, 4, and 14 have been canceled. Furthermore, Applicants submit that none of the newly-added claims correspond to previous claims 1, 4, and 14. Therefore, Applicants submit that the rejections of claims 1, 4, and 14 are moot and respectfully request withdrawal thereof.

Nevertheless, Applicants wish to further point out differences between the cited art and the present claimed invention by the below explanations.

One non-limiting feature of the present claimed invention forms a bonded wafer body by bonding an active layer wafer and a supporting wafer together. A part of the active layer wafer that is included in the bonded wafer body is thinned down to form an SOI layer. Therefore, an SOI wafer has the SOI layer on the supporting wafer via an insulating film. This SOI layer is used as a device forming layer. The present specification clearly describes each element of the subject matter (shown, *e.g.*, in paragraph [0009] at page 5).

The present invention as recited in claim 18 provides a method for manufacturing an SOI wafer comprising bonding an active layer wafer with a supporting wafer via an insulating film to form a bonded wafer body; reducing a film thickness in a part of the active layer wafer that forms a part of the bonded wafer body to form an SOI layer for manufacturing the SOI wafer, wherein the supporting wafer has a nitrogen concentration in a range of $1x10^{14}$ atoms/cm^3 to $3x10^{15}$ atoms/cm^3 and an oxygen concentration of equal to or higher than $12x10^{17}$ atoms/cm^3 when measured in accordance with old ASTM so as to have an oxidation induced stacking fault substantially entirely across a surface thereof.

In accordance with a non-limiting feature of the invention, when using the above-claimed configuration, when heat processing is performed after the wafers are bonded, Cu, Fe, and the like of the metal impurities that are contained in the active layer wafer diffuse outward and are captured by an oxide deposit Bulk Micro Defects (BMD) in the supporting wafer or by an oxidation induced stacking fault OSF that originates from the

BMD. Cu, Fe, and the like that are present in the supporting wafer and that move to the active layer wafer or to the SOI layer through a buried insulating film are captured by Crystal Originated Pits (COP) or the Oxidation induced Stacking Fault (OSF) (defect) in a similar manner. Other metal impurities in the supporting wafer are also captured by this defect. Consequently, contamination of the SOI layer due to the metal impurities can be reduced.

A bonded wafer that has the above-described effects can be obtained by adding a predetermined amount of nitrogen and oxygen, or oxygen alone in a crystal when an ingot for the supporting wafer is pulled up. Consequently, the bonded wafer having the above-described effects can be manufactured at low cost.

Further, in accordance with a non-limiting feature of the present claimed invention described in claim 19, a method is provided for manufacturing an SOI wafer comprising bonding an active layer wafer with a supporting wafer via an insulating film to form a bonded wafer body; and reducing a film thickness in a part of the active layer wafer that forms a part of the bonded wafer body to form an SOI layer for manufacturing the SOI wafer, wherein the supporting wafer has an oxygen concentration of equal to or higher than $16x10^{17}$ atoms/cm^3 when measured in accordance with old ASTM. Also in accordance with a non-limiting feature of claim 19, the supporting wafer has an oxygen concentration of equal to or higher than $16x10^{17}$ atoms/cm^3, which results in a defect density of the supporting wafer equal to or higher than $1x10^9$/cm^3 without the addition of nitrogen.

When using the above-claimed configuration, in addition to the gettering function of the above-described supporting wafer in accordance with, *inter alia*, paragraph [0015]

of the specification, when the oxygen concentration reaches a value of equal to or higher than $16x10^{17}$ atoms/cm^3, a BMD density shows a value sufficient to suppress the occurrence of slip. As a result, the mechanical strength of the supporting wafer is enhanced, thereby preventing the occurrence of slip in the supporting wafer during the heat treatment.

The bonded wafer according to a non-limiting feature of the present invention can be obtained simply by adding oxygen of equal to or higher than $16x10^{17}$ atoms/cm^3 in a crystal when an ingot for the supporting wafer is pulled up. Consequently, the bonded wafer having the above-described effect can be manufactured at low cost.

In contrast to the present claimed invention of independent claims 18-19, Tamatsuka discloses a thin film SOI substrate including an SOI layer having a thickness of 1μm or less and a manufacturing method thereof. According to the manufacturing method, nitrogen-doped wafers are bonded together so as to fabricate an SOI substrate including an SOY layer having a thickness of 0.2μm through steps such as grinding, polishing, and vapor-phase etching.

In addition, Falster describes that a supporting wafer has certain types of dislocations and stacking faults that act as intrinsic gettering as opposed to the above described gettering. Specifically, the present invention exhibits each effect such as gettering, prevention of an occurrence of slip in a supporting wafer, easy Light Point Defect (LPD) evaluation, and reduction of manufacturing costs, as a result that the supporting wafer is given nitrogen and oxygen of a predetermined concentration range so as to produce an OSF across an entire surface thereof, as generally recited in independent claim 18.

Further, neither Tamatsuka nor Falster discloses or renders obvious at least concentration ranges of nitrogen and oxygen in a supporting wafer that is included in the present claimed invention. Moreover, there is no cited teaching that an SOI wafer is manufactured by using, as a supporting wafer, a wafer in which an OSF has occurred due to such nitrogen and oxygen of a predetermined concentration range, as generally recited in independent claim 19. Therefore, Tamatsuka nor Falster fail to qualify as a prior art reference to at least the independent claims of the present invention

With respect to the Examiner's rejection of the dependent claims, Applicants submit that newly-submitted dependent claims 20-33 are dependent from one of allowable independent claims 18 and 19, which are each allowable for at least the reasons discussed *supra*. Thus, these dependent claims are also allowable for at least the reasons discussed *supra*. Further, these dependent claims set forth a further combination of elements neither taught nor disclosed by any of the applied references, as noted in the below examples.

For example, neither Tamatsuka nor Falster disclose at least the ion-implanting of hydrogen gas or a noble gas element to the active layer wafer to form an ion-implanted layer in the active layer wafer as recited in dependent claims 20 and 21; or a thickness of the SOI layer is thinner than 0.10 μm as recited in dependent claims 22 to 25; or applying a rapid thermal process at a temperature in a range of 1100 °C to 1250 °C for five minutes or longer to the supporting wafer in a reducing gas atmosphere, prior to said bonding, or applying a high-temperature heat treatment at a temperature in a range of 1050 °C to 1250 °C for one hour or longer to the supporting wafer in a reducing gas atmosphere, prior to said bonding, as generally recited in dependent claims 26 to 33.

For example, a non-limiting feature of the present invention described in claim 20 provides a method for manufacturing an SOI wafer in accordance with claim 18, further comprising

ion-implanting of hydrogen gas or a noble gas element to the active layer wafer to form an ion-implanted layer in the active layer wafer, prior to said bonding; and heat treating the bonded wafer body to thereby induce cleavage in the bonded wafer body at the site of the ion-implanted layer as an interface so as to form the SOI layer with a remaining active layer.

The present invention described in claim 21 provides a method for manufacturing an SOI wafer in accordance with claim 19, further comprising ion-implanting of hydrogen gas or a noble gas element to the active layer wafer to form an ion-implanted layer in the active layer wafer, prior to said bonding; and heat treating the bonded wafer body to thereby induce cleavage in the bonded wafer body at the site of the ion-implanted layer as an interface so as to form the SOI layer with a remaining active layer.

In addition to the above-described effects, the present invention includes simplified manufacturing of an SOI wafer.

As generally recited in the dependent claims, before bonding, rapid thermal processing at a temperature in a range of 1100 °C to 1250 °C for five minutes or longer, or a high-temperature heat treatment at a temperature in a range of 1050 °C to 1250 °C for one hour or longer is applied to the supporting wafer, in a reducing gas atmosphere, which facilitates the outward diffusion of the oxygen that is present in the vicinity of the front and the back surfaces of the supporting wafer, so that the oxygen diffuses outward from the front and the back surfaces of the wafer.

Accordingly, the oxide film (inner wall oxide film) of the inner surface of the COP that is present in the vicinity of the wafer surface is unsaturated and dissolved. The COP whose inner wall oxide film is annihilated is filled with the interstitial silicon that is present in the peripheral region, causing the COP to disappear. There is no crystal defect present in the supporting wafer.

Consequently, even if the SOI layer and the buried insulating film are thinned down to such an extent that a laser light for LPD evaluation can pass through the layer and the film respectively, the LPD evaluation never detects the micro void (COP) that exists between the buried insulating film and the supporting wafer as a pseudo defect. Therefore, the reliability of the LPD evaluation of the active layer can be enhanced.

Thus, Applicants respectfully submit that each and every pending claim of the present application meets the requirements for Patentability at least under 35 U.S.C. § 103, and respectfully request the Examiner to indicate the allowance of each and every pending claim in the present application.

SUMMARY AND CONCLUSION

In view of the fact that none of the art of record, whether considered alone, or in any proper combination thereof, discloses or otherwise renders unpatentable the present invention, reconsideration of the Examiner's action and allowance of the present application are respectfully requested and are believed to be appropriate.

Applicants note that this amendment is being made to advance prosecution of the application to allowance, and should not be considered as surrendering equivalents of the territory between the claims prior to the present amendment and the amended claims.

Further, no acquiescence as to the propriety of the Examiner's rejection is made by the present amendment. All other amendments to the claims which have been made in this amendment, and which have not been specifically noted to overcome a rejection based upon the prior art, should be considered to have been made for a purpose unrelated to patentability, and no estoppel should be deemed to attach thereto.

Should there be any questions, the Examiner is invited to contact the undersigned at the below-listed telephone number.

Respectfully Submitted
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Attachment: Fumio SHIMURA, "Semiconductor and Silicon Crystal Technology", Academic Press, Inc., San Diego, New York, Berkeley, Boston, London, Sydney, Tokyo, Toronto, 1989, pp. ii-viii, 1, 232-233, and 274-275; and

Form PTO-1449 listing the enclosed document

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